IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Jason GOSIOR et al.
Assignee:	ELEVEN ENGINEERING INC.
Patent No.	7,320,065
Issue Date:	January 15, 2008
Application No.:	09/843,178
Filing Date:	04/26/2001
Title:	MULTITHREAD EMBEDDED PROCESSOR WITH INPUT/OUTPUT CAPABILITY
Group Art Unit:	2183
Examiner:	Li, Aimee J.
Attorney Docket No.:	116.003
Customer No.:	31209

REQUEST FOR EXPEDITED ISSUANCE OF

CERTIFICATE OF CORRECTION UNDER 37 C.F.R. 1.322

January 22, 2008 **FILED VIA EFS-Web**

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION - EXPEDITED ISSUANCE

Upon a review of Patent No. 7,320,065 in light of the prosecution history, it is apparent that the patent contains certain printing errors which require correction in order to conform with the official record in the application. Accordingly, issuance of a Certificate of Correction is requested pursuant to 37 C.F.R. 1.322.

Nature of Errors

The Notice of Allowability dated September 25, 2007 (and mailed with the Notice of Allowance dated October 5, 2007) included an Examiner's Amendment which made wording changes in three sub-paragraphs in Claim 1. The Examiner's Amendment recited only the claim preamble and the three affected sub-paragraphs, and included ellipses (. . .) to indicate the presence of additional text not affected by the Examiner's Amendment. In Patent No. 7,320,065, as published on January 15, 2008, Claim 1 was printed with only the preamble and the three amended sub-paragraphs (as well as ellipses from the Examiner's Amendment). As a result, a total of seven (7) sub-paragraphs are missing from Claim 1 as published.

Documents Enclosed

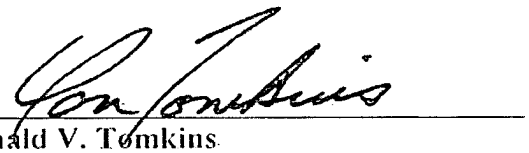
The enclosed Form PTO/SB/44 (Certificate of Correction) seeks to correct the aforesaid printing errors by deleting the entirety of Claim 1 as published, and replacing it with the complete text of Claim 1 in accordance with the Examiner's Amendment. Also enclosed in support of the requested Certificate of Correction are copies of the following documents from the prosecution of the corresponding Application No. 09/843,178:

- Amendment and Response to Non-Final Action (filed July 26, 2007); and
- Notice of Allowability (mailed September 25, 2007, and responsive to the amendment filed July 26, 2007), with Examiner's Amendment.

Expedited Issuance of Certificate of Correction Requested

In accordance with the foregoing, it is respectfully submitted that the errors sought to be corrected by issuance of a Certificate of Correction arose during the process of printing the letters patent, and that the requested Certificate of Correction should therefore be issued under 37 CFR 1.322, without charge to the patentee. It is further submitted that the present submission and accompanying documentation meet the requirements for expedited issuance of the requested Certificate of Correction for errors attributable solely to the USPTO, per MPEP § 1480.01, and expedited issuance of the Certificate of Correction is hereby requested.

Respectfully submitted on behalf of the
Assignee, **Eleven Engineering Inc.**,
by its agent:



Donald V. Tomkins
Registration No. 48,206
Customer No. 31209

c/o TOMKINS LAW OFFICE
Suite 740, 10150 - 100 Street
Edmonton, Alberta, CANADA
T5J 0P6

Telephone: (780) 424-2200
Facsimile: (780) 424-2205

E-mail: dtomkins@tomkinslaw.ca

Enclosures:

1. Form PTO/SB/44 – Certificate of Correction;
2. Amendment and Response to Non-Final Action (filed July 26, 2007); and
3. Notice of Allowability (Sept. 25, 2007), with Examiner's Amendment.

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,320,065

APPLICATION NO.: 09/843,178

ISSUE DATE : January 15, 2008

INVENTOR(S) : Jason GOSIOR, Colin BROUGHTON, Phillip JACOBSEN, and John SOBOTA

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 20, delete text beginning at line 2 with "1. A programmable, single-chip" to and including "(5) . . ." at column 20, line 19, and insert therefor:

--1. A programmable, single-chip embedded processor comprising:
(a) a multiple-bit, multithreaded processor core comprising a single processor pipeline having a 'k' number of pipeline stages shared by one or more independent processor threads, the number 'k' being equal to at least four, and a number 'n' of said processor threads being equal to or less than 'k';
(b) an instruction execution logic mechanism engaged with said processor core for executing instructions from a built-in instruction set;
(c) a supervisory control unit, controlled by one or more control threads selected from said processor threads, for examining the processor core state and for controlling the operation of said processor core, said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation;
(d) a memory capable of storing data comprising instructions from said instruction set, said memory being internally integral to the embedded processor, and comprising a main RAM and a boot ROM; and
(e) a peripheral adaptor internally integral to the embedded processor and engaged with said processor core for transmitting input/output signals to and from said processor core;
wherein:
(f) each of the 'n' program threads occupies a unique pipeline stage at any given time;
(g) each program thread advances to the next pipeline stage with every clock cycle;
(h) for a given program thread, the pipeline completes a one-word instruction every 'k' clock cycles;
(i) a first selected program thread is adapted to wait for a specified number of clock cycles for a response from a designated peripheral device; and
(j) a second selected program thread is adapted to re-initialize said first selected program thread if the designated peripheral device does not respond within the specified number of clock cycles.--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Donald V. Tomkins
#740, 10150 - 100 Street
Edmonton, AB, Canada T5J 0P6

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	**Jason GOSIOR et al.**
Serial No.:	09/843,178
Filing Date:	04/26/2001
Title:	**MULTITHREAD EMBEDDED PROCESSOR WITH INPUT/OUTPUT CAPABILITY**
Group Art Unit:	2183
Examiner:	Li, Aimee J.
Attorney Docket No.:	116.003
Customer No.:	31209

AMENDMENT AND RESPONSE TO

NON-FINAL ACTION MAILED JANUARY 29, 2007

July 26, 2007 **FILED VIA EFS-Web**

TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

A. INTRODUCTORY COMMENTS

1. Amendment Filed With Petition for Three-Month Extension

The present amendment is in response to the Non-Final Action mailed January 29, 2007. Accordingly, the present amendment is being filed within the statutory reply period. Since the shortened three-month statutory period for reply ended on April 29, 2007, the present amendment is accompanied by a petition for a three-month extension pursuant to 37 CFR 1.136(a). Payment of the extension fee under 37 CFR 1.17(a)(3) is being submitted concurrently with the EFS-Web filing of the present amendment.

2. Amendments to the Application

Applicants respectfully request entry of the amendments set out below, and consideration of the accompanying remarks, as follows:

(a) Amendments to the claims in accordance with the listing of claims which begins on page 3 of this paper; and

(b) Remarks as set out beginning on page 7 of this paper.

B. AMENDMENTS TO THE CLAIMS

Please amend the claims in accordance with the following complete listing of all claims in the application:

Claim 1 (currently amended): A programmable, single-chip embedded processor comprising:

(a) a multiple-bit, multithread processor core comprising a single processor pipeline having 'k' pipeline stages shared by one or more independent processor threads, the number 'k' being equal to at least four, and the number 'n' of said processor threads being equal to or less than 'k';

(b) an instruction execution logic mechanism engaged with said processor core for executing instructions from a built-in instruction set;

(c) a supervisory control unit, controlled by one or more control threads selected from said processor threads, for examining the processor core state and for controlling the operation of said processor core, said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation;

(d) a memory capable of storing data comprising instructions from said instruction set, said memory being internally integral to the processor, and comprising a main RAM and a boot ROM; and

(e) a peripheral adaptor internally integral to the processor and engaged with said processor core for transmitting input/output signals to and from said processor core;

wherein:

(f) each of the 'n' program threads occupies a unique pipeline stage at any given time;

(g) each program thread advances to the next pipeline stage with every clock cycle; ~~and~~

(h) for a given program thread, the pipeline completes a one-word instruction every 'k' clock ~~cycles.~~ cycles;

(i) a first selected program thread is adapted to wait for a specified number of clock cycles for a response from a designated peripheral device; and

(j) a second selected program thread is adapted to re-initialize said first selected program thread if the designated peripheral device does not respond within the specified number of clock cycles.

Claim 2 (previously presented): An embedded processor as recited in Claim 1, wherein said processor pipeline includes an instruction fetch logic stage, an instruction decode logic stage, a multiple port register read stage, an address mode logic stage, an arithmetic logic unit for arithmetic and address calculations stage, a multiple port memory stage, a branch/wait logic stage, and a multiple port register write stage.

Claim 3 (previously presented): An embedded processor as recited in Claim 1, wherein said processor core supports one or more additional independent groups of at least two processor threads, each group of processor threads being associated with an instruction execution logic mechanism and a memory.

Claim 4 (previously presented): An embedded processor as recited in Claim 1, further comprising a condition code mechanism implemented in said instruction set for detecting specific word data types.

Claim 5 (previously presented): An embedded processor as recited in Claim 4, wherein the value of the least significant byte of a word is detected to be within a specific range.

Claim 6 (previously presented): An embedded processor as recited in Claim 1, wherein said instruction set includes a processor instruction for enabling individual program threads to identify the particular processor threads on which they are being executed.

Claim 7 (previously presented): An embedded processor as recited in Claim 1, wherein said supervisory control unit is capable of examining, interpreting, and adjusting the state of the processor core for the purpose of starting and stopping individual processor threads, and modifying the state of each individual processor thread.

Claim 8 (previously presented): An embedded processor as recited in Claim 7, further comprising a hardware semaphore vector engaged with said supervisory control unit for controlling multithread access to said peripheral adaptor and said memory.

Claim 9 (previously presented): An embedded processor as recited in Claim 1, wherein said supervisory control unit is capable of being accessed and controlled by one or more controlling threads selected from the processor threads in the processor core, by using input/output instructions to control the operation of one or more processor threads.

Claim 10 (previously presented): An embedded processor as recited in Claim 9, wherein said one or more controlling threads are programmable.

Claim 11 (previously presented): An embedded processor as recited in Claim 9, wherein said one or more controlling threads are capable of reconfiguring the overall thread processing method of operation so that two or more processor threads can support MIMD operations.

Claim 12 (previously presented): An embedded processor as recited in Claim 9, wherein said one or more controlling threads can reconfigure the overall thread processing method of operation so that two or more processor threads can support SIMD operations.

Claim 13 (previously presented): An embedded processor as recited in Claim 9, wherein said one or more controlling threads are capable of reconfiguring the overall thread processing method of operation so that two or more processor threads can support simultaneously SIMD operations, and two or more processor threads can support MIMD operations.

Claim 14 (previously presented): An embedded processor as recited in Claim 1, wherein said supervisory control unit is operable by a first processor thread to start and stop the operation of another processor thread and to examine and alter processor core state information in single-step and multiple-step modes of controlled operation.

Claim 15 (previously presented): An embedded processor as recited in Claim 1, further comprising an identifying bit pattern embedded in said instruction set.

Claim 16 (previously presented): An embedded processor as recited in Claim 1, wherein said memory is expandable by addition of external memory accessible by the system through said peripheral adaptor.

Claim 17 (previously presented): An embedded processor as recited in Claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core.

Claim 18 (previously presented): An embedded processor as recited in Claim 1, wherein said peripheral adaptor is capable of controlling analog and digital processing functions.

Claim 19 (previously presented): An embedded processor as recited in Claim 15, wherein said identifying bit pattern is used to identify programming code for code protection purposes.

Claim 20 (previously presented): An embedded processor as recited in Claim 15, wherein said identifying bit pattern does not affect the operation of the instruction execution logic mechanism.

Upon entry of the proposed amendments, the claims pending in the application will be **Claims 1-20.**

C. REMARKS

1. Amendments to the Claims

Claim 1 has been amended to add the limitations correct the informality (punctuation error) identified in ¶ 3 of the Final Action.

2. Claim Rejections on Grounds of Obviousness under 35 U.S.C. § 103

In the Non-Final Action dated January 29, 2007, the Examiner rejected Claim 1 for obviousness based on the Li reference ("The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE © 1995) in view of the ARM reference (Furber: "ARM System-on-Chip Architecture", Second Edition © 2000). In the current amendment, new sub-paragraphs (i) and (j) have been added to Claim 1 to introduce a "wait" feature whereby the operation of a given program thread may be stalled, or its operation resumed, based on the internal state of a peripheral device. Applicants submit that this feature is not taught by either the Li reference or the ARM reference. It follows that Claim 1, as currently amended, is not obvious in view of Li and ARM, and is therefore allowable. Because Claims 2-20 are dependent from Claim 1, either directly or indirectly, it also follows that Claims 2-20 are non-obvious and allowable.

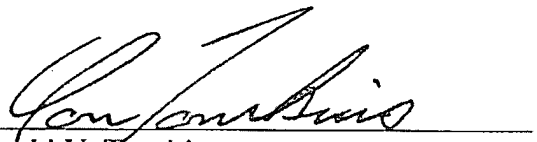
3. No New Matter

It is submitted that the current amendments introduce no new matter into the application. All subject matter contained in the application, as currently amended, was expressly described in or is reasonably inferable from the originally-filed specification, claims, abstract, and/or drawings. More specifically, support for the limitations added to Claim 1 by virtue of the current amendments may be found in paragraph [0038] of the specification as originally filed (per Pub. No. US 2003/0093655).

D. CONCLUDING REMARKS

Applicants respectfully submit that the amendments and remarks presented herein have fully addressed all issues raised in the Non-Final Action dated January 29, 2007, and that the application will be in condition for allowance upon entry of the amendments. Accordingly, Applicants request timely issuance of a Notice of Allowance.

Respectfully submitted on behalf of the Applicants, by their agent:



Donald V. Tomkins
Registration No. 48,206
Customer No. 31209

c/o TOMKINS LAW OFFICE
Suite 740, 10150 - 100 Street
Edmonton, Alberta, CANADA
T5J 0P6

Telephone: (780) 424-2200
Facsimile: (780) 424-2205

E-mail: dtomkins@tomkinslaw.ca

Enclosures:

1. Petition for three-month extension [1 page].

Notice of Allowability	Application No.	Applicant(s)	
	09/843,178	GOSIOR ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 26 July 2007*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 7/26/2007
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Donald Tomkins (Reg. No. 48,206) on 28 September 2007.

3. The application has been amended as follows: Added language is underlined and deleted language is indicated with double brackets.

a. Claim 1:

i. A programmable, single-chip embedded processor comprising:

(1) A multiple-bit, multithread**ed** processor core comprising a single processor pipeline have **a** 'k' **number of** pipeline stages shared by one or more independent processor threads, the number 'k' being equal to at least four, and **[[the]]a** number 'n' of said processor threads being equal to or less than 'k';

(2) ...

(3) A memory capable of storing data comprising instructions from said instruction set, said memory being internally integral to the **embedded** processor and comprising a main RAM and a boot ROM; and

(4) A peripheral adaptor internally integral to the **embedded** processor and engaged with said processor core for transmitting input/output signals to and from said processor core;

(5) ...

b. Claims 2-20:

i. **[[An]]The** embedded processor as recited in...

REASONS FOR ALLOWANCE

4. The following is an examiner's statement of reasons for allowance: Applicants have amended the claims to add the limitations "a first selected program thread is adapted to wait for a specified number of clock cycles for a response from a designated peripheral device; and a second selected program thread is adapted to re-initialize said first selected program thread if the designate peripheral device does not respond within the specified number of clock cycles." While the prior art searched does teach a thread waiting a specified number of clock cycles for response from a designated peripheral device, it does not teach a second program thread to re-initialize the waiting program thread when the specified number of clock cycles has been passed. The prior art searched and found has taught either the waiting thread switches to another thread or the waiting thread re-starts the waiting period. The prior art does not teach a separate second thread re-starting the waiting thread from the beginning with the beginning values, as is claimed by the language "a second selected program thread is adapted to re-initialize said first selected program thread".

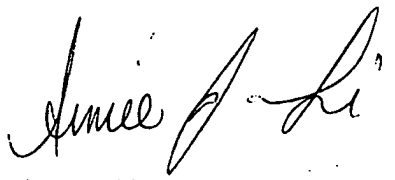
5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Aimee J Li
Examiner
Art Unit 2183

25 September 2007